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AI-Guided Hybrid Power Optimization for VLSI: Combining Clock Gating, Power Gating, DVFS, and MTCMOS in Embedded Systems

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Abstract: *The rapidly growing applications of embedded systems in mobile devices, Internet of Things (IoT), and wearables technologies now require the design of low-power Very-Large-Scale Integration (VLSI) circuits to manage the power consumption demand of semiconductor devices used in different electronic circuits. To reduce power consumption and maintain system-level performance/functionalities in designing a VLSI circuit, various techniques are developed, among the most effective are: (1)Clock Gating, (2)Power Gating, (3) Dynamic Voltage and Frequency Scaling (DVFS), and (4)Multi-Threshold CMOS (MTCMOS). These techniques feature in actively disabling the clock signal in the inactive portion of the circuit, the isolation of inactive blocks, tweaking voltage and frequency to match workload demands to reduce dynamic power dissipation, and minimizing leakage power (when the circuit is idle) by using transistors with different threshold voltages to minimize the power dissipation. However, the individual usage of these four techniques improves one parameter and disturbs other parameters (for e.g.,* ***Clock Gating*** *saves dynamic power but doesn't help much with leakage.* ***Power Gating*** *saves leakage but increases area (extra sleep transistors) and can cause delay when waking up.****DVFS*** *reduces dynamic power but can reduce performance if the voltage/frequency is lowered too much.* ***MTCMOS*** *reduces leakage but adds complexity/area overhead. In order to overcome all the above limitations, this research paper proposes an AI-driven hybrid power optimization framework that combines all the above four techniques and, according to the system requirements, uses them independently or in combination. The Reinforcement learning (RL) AI model is used that monitors the system workload, switching activity, and thermal conditions, and intelligently selects the four techniques in real time to have the best possible energy efficiency results. The performance of the proposed framework is tested on VLSI-EDA tools (Synopsys-Primetime PX) to measure the dynamic power, leakage power, and performance/area trade-offs. The results show that the proposed framework is a good indication for use in future embedded devices and can offer innovation opportunities as the AI-based future innovation opportunities for low-power design techniques have become a fundamental demand of VLSI designers due to the increase in energy-efficient demand.*

Keywords: *Low-power VLSI design, clock gating, power gating, dynamic voltage and frequency scaling (DVFS), multi-threshold CMOS (MTCMOS), Reinforcement Learning embedded systems, power dissipation, energy efficiency, performance trade-offs, power optimization techniques, static power, dynamic power, system modeling, gate-level synthesis*

1. Introduction

As technology develops rapidly, the demand for energy-efficient systems is becoming more important. The field of Very Large-Scale Integration (VLSI) design is essential for the production of ICs, which act as the prime components of electronic devices. The increasing design constraint for circuitry is power consumption, and this is thanks to transistors getting smaller and more components being added to chips. Batteries have become an essential requirement for a mobile device as well as for many other devices, including IoT. In these applications, efficient power management is necessary because they have to work for long periods of time and not recharge frequently [1]. VLSI design involves grouping power consumption into 2 types, namely dynamic power and static power, as explained below. Due to the switching of transistors, faults are blamed for losing power. Dynamic power dissipation is the term used to refer to this type of power loss. On the one hand, leakage currents cause static power dissipation. This is more important as transistors get smaller. Leakage used when the load is inactive or lightly active consumes a large portion of total power in modern deep-submicron technologies [2]. The challenges we meet nowadays lead to the development of low-power VLSI design techniques that have less dynamic and static power dissipation with the same performance level of the system [3]. Many different techniques have been used to address various angles of power consumption. The overall issue includes power optimization in a VLSI circuit. Chakraborty and other people have studied and implemented gate techniques like clock gating, power gating, and DVFS, i.e., dynamic voltage and frequency scaling. Clock gating is a technique used to reduce power consumption. The clock signal is turned off in the circuits that are not active or idle. As a result, it stops excess switching activity and lowers dynamic power wastage [4-5]. So, power gating can cut off power from the sections that are unused in the circuit, which considerably reduces the leakage power [6]. According to [7], DVFS adjusts the power supply together with the clock rate of a circuit. During less activity, it makes power savings. MTCMOS is a technique widely used in CMOS circuits for power reduction. It does this by utilizing transistors with different threshold voltages to block leakage currents. While it is true that these techniques can lead to less power being used, they do also bring problems. As stated in [8], clever control logic is needed to turn off the clock only at times when it is safe to do so. Power gating uses more area for adding sleep transistors. Also, DVFS has large performance penalties on large performance applications [9]. To ensure efficient energy consumption in embedded systems, there is a need to optimally manage trade-offs between power, performance, and area [10]. The need of the hour is intelligence, i.e., embedded intelligent systems, which need to be designed and developed. Approximate computing is a newer computing paradigm where some degree of deviation in computational accuracy is permitted in exchange for significant power savings. This is especially useful in less critical applications. Also, quantum-dot transistors, spintronics, memristor computing, and others are being explored. According to [11-12], reducing power dissipation has the potential to achieve high performance.

The aim of the paper is to provide an overview of the significant techniques used in the low-power VLSI circuit design and their application in Embedded Systems. Simulations and comparisons will be used to showcase the advantages and disadvantages of those techniques as well as the directions for future development. Similarly, the article will look at the trade-offs between power, performance, and area in future-generation embedded systems. It will also provide insight into how to optimize these design considerations to meet modern application requirements.

1.1. Research objectives

1- To evaluate the constraints of current techniques to design low-power VLSI design methods like clock gating, power gating, DVFS, and MTCMOS used alone.
2- To come up with a hybrid low-power VLSI architecture that combines these methods to attain dynamic and leakage power savings without compromising system performance.
3- To create a reinforcement learning (RL) based AI-driven power management controller to dynamically select and combine low-power techniques in response to changing workloads.
4- To assess the proposed solution with the help of gate-level simulation and power analysis software for embedded and IoT system workloads.
5- The objective function is explained in Eq. A (that is, to minimize the total power/cost under workload and thermal constraints)

$$F= w_1(\alpha C_{load}V^2f) + w_2 (I_{leak} V) + w_3 A + w_4D + w_5T - w_6\frac{Perf(f)}{P_{DYN}+P_{leak}} + w_7 (1-R)(A)$$

Where $P_{DYN} = (\alpha C_{load}V^2f)$ dynamic power, $P_{leak} = (I_{leak} V)$ leaking power, A = area overhead, D= delay penalty, T= temperature, R=reliability factor, and w_i= weighting coefficient.

1.2. Highlights of the Research

1. The Hybrid Power Optimization Framework: Presented the initial unified VLSI design flow, which integrates clock gating, power gating, DVFS, and MTCMOS into one control mechanism.
2. RL-Based Controller: Developed an AI-based decision engine that dynamically chooses low-power strategies and tunes these based on real-time workload, activity, and thermal conditions.
3. Workload-Aware Adaptability: Illustrated the way RL can accommodate heterogeneous workloads (IoT, mobile, wearable applications) to provide the best power savings without performance loss.
4. Simulation & Validation: Performed power simulations and gate-level synthesis with industry-standard EDA (e.g., Synopsys PrimeTime PX) to test the framework.

The working model of the proposed AI-based VLSI framework is shown in Figure 1

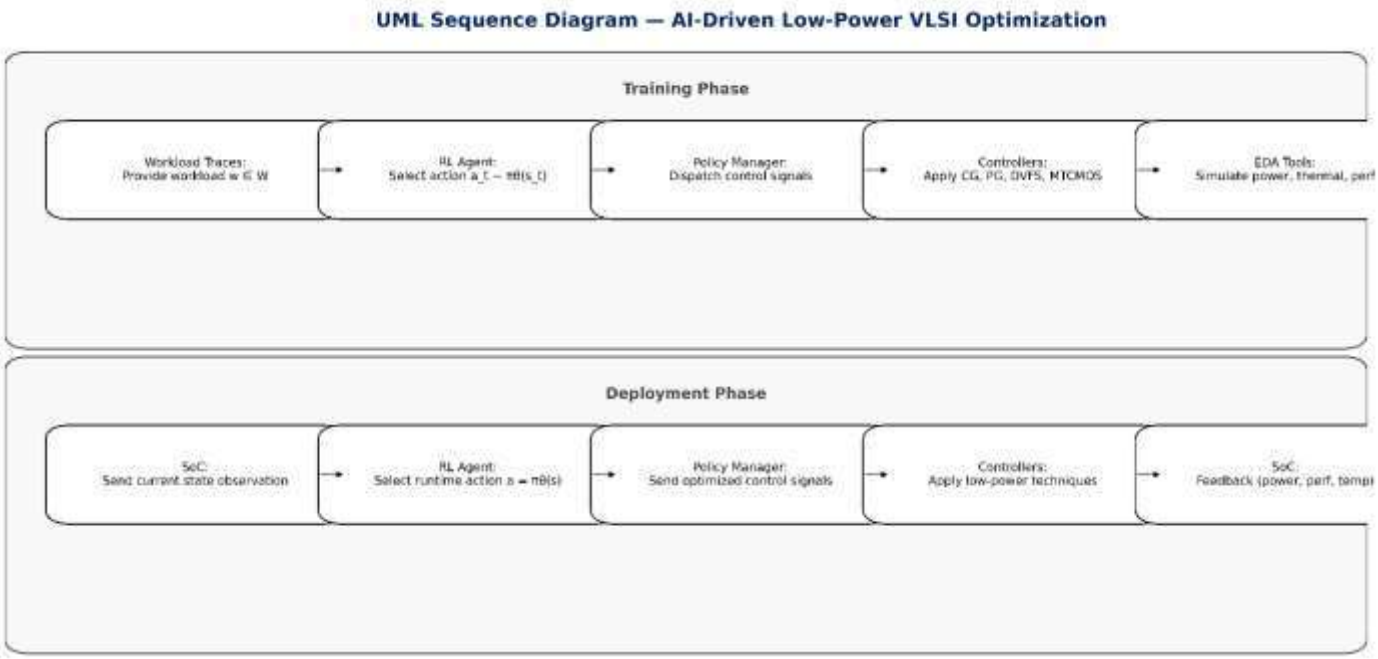

Figure 1: UML working model of proposed AI-based VLSI framework

2. Literature Review:

2.1. Introduction to Low-Power VLSI Design

As power requirements increase, there is a need for low-power design of VLSI circuits for low-power applications. To be precise, specialists in embedded systems are designing VLSI circuits that consume less power. Chips now contain millions of transistors as VLSI technology improves. Consequently, this trend is forcing circuit designers to push the envelope in performance, area, power consumption, and other areas. With the proliferation of smaller and more efficient devices in the modern world, effective management of all the power it requires has also become a significant factor [13]. Earlier, the key issues for VLSI designs were improving performance and minimizing area. With the introduction of mobile, battery-operated, and wireless devices, power (the third P) consumption is now one of the most critical design parameters. These days, low-power and efficient systems are very much essential, and they should be checked out for less power to perform.

2.2. Power Consumption in VLSI Circuits

VLSI circuits consume power during dynamic power dissipation and static (leakage) power dissipation. Discharging dynamic power is the dissipating power when transistors switch states. When this happens, it consumes power. While charging and discharging, all the power is dissipated dynamically. This type's power dissipation is a function of operational frequency, supply voltage, and capacitance [14]. Grant application language should, unless otherwise stated, be arranged as follows: Static power dissipation is owing to leakage currents and has now become a serious problem as the devices become smaller and threshold voltages of transistors [15]. As technology scales down, leakage power will become a major contributor to power dissipation in ICs. Consequently, dynamic power dissipation and static power dissipation must be considered in a VLSI circuit's low-power design.

2.3. Techniques for Power Optimization in VLSI Circuits

To lessen power consumption in VLSI, numerous techniques have been developed. The techniques can be divided into three methods: those that reduce the dynamic power, static power, and energy consumption.

2.4. Clock Gating

The method of clock gating prevents the propagation of an undesired clock signal in the sequential circuit. It lessens the switching movement of circuits that you disable by shutting off their clock signals. If you use this technique, it can result in larger dynamic power reductions for large complex systems. Only part of the circuit will ever be active [16]. To do this, the clock signal must be controlled so that only types of idle sections get gated in the circuit and not active ones.

2.5. Power Gating

VLSI circuits employ power gating to achieve further reductions in power dissipation. Disconnection of inactive blocks from the power supply by making use of high threshold voltage transistors to prevent leakage power [17] is the technique. Deep submicron technologies have large leakage currents, so power gating is used. Power gating involves adding new circuits, referred to as sleep transistors, that modify the power supply state so it does not interfere with the circuit functioning, despite the sleep transistors behaving as the faulty power supply. Also, extra latency into state transitions added by power gating [18] impacts performance.

2.5. Dynamic Voltage and Frequency Scaling (DVFS)

Changing voltage and frequency means dynamic voltage and frequency scaling (DVFS). The voltage and frequency (i.e., clockwise speed) of the circuit are changed dynamically based on the load. Reducing voltage and frequency during off-peak hours can save a considerable amount on power consumption at a system performance cost. Processors and embedded systems use DVFS [19]. Most battery-powered devices use a lithium-ion battery. It might be

a mobile or a laptop. Even so, the power saving-performance trade-off is also a challenge to get to the point where power consumption can be reduced without degrading the user experience [20-21].

2.6. Multi-Threshold CMOS (MTCMOS)

MTCMOS is a new technology that aims to reduce dynamic power and leakage by using transistors with zero bias and different threshold voltages in a given circuit. The use of high-threshold voltage transistors that are placed in non-critical high-performance areas will minimize leakage current. On the flip side, fast operation-relevant area in MTCMOS uses low-threshold voltage transistors. Studies have been conducted to analyze the performance of the MTCMOS technique on a given circuit. Using negative feedback can help in stabilizing gain and other design parameters. However, it can complicate the design. Correlating circuit performance with transistor threshold voltages (VTs) requires improved control.

2.7. Approximate Computing

Approximate computing is a low-power VLSI design. It allows you to save energy with an error margin in the results. Using approximate computing can be helpful for applications where precision is not a priority. Image processing, machine learning, and multimedia applications can use it effectively [22]. Approximate computing can improve the power efficiency of embedded systems. This method can help next-gen systems because their accuracy requirement do not need to be too strict. For example, approximation to a greater degree has to be controlled to avoid losing the effectiveness of the system, etc.

2.8. Emerging Technologies in Low-Power VLSI Design

Different research centers are working on different low-power design methods, Techniques like QDot transistors, memristors, and spintronics. Transistors that use quantum dots rely on quantum physics principles to improve their switching speed and decrease their power loss compared with CMOS transistors [23] .A research study will help achieve faster and energy-efficient circuits through the aid of spintronics. According to [24], using memristors could allow us to have non-volatile memory options that would lessen the energy overhead of traditional memory systems. The low-power VLSI design experts have given predictions that these technologies may be a game-changer for low-power VLSI design.

2.9. Challenges and Future Directions

Though modern-day low-power VLSI design techniques are beneficial, some difficulties arise. The ongoing innovative development of semiconductors is a real problem for electric power. Power leakage will be the major contributor to 22 nm process nodes and below [25-26]. When you combine many low-power techniques together, it involves a complex design trade-off in terms of power, performance, and area. In order to achieve maximum power

efficiency, the load request and technique implemented should conform to the design. Future projects on low-power VLSI design will include new power techniques adopted by programmers. Machine learning can be used to customize the controller in an adaptive manner using new materials and devices, including graphene and carbon nanotubes [27]. Portable applications will require the integration of high-performance computing along with low power consumption. The next generation of embedded devices may optimize power consumption using 3D integration and heterogeneous computing architectures. VLSI design for low power is becoming a necessity due to the expansion of embedded systems. As the years progressed, the energy consumption of the circuit due to dynamic and static power dissipation increased continuously. You can minimize your power dissipation through clock gating, power gating, dynamic voltage scaling, and multiple threshold CMOS techniques. Reduction of technology presents opportunities and obstacles for business. This will lead us to emerging technologies and paradigms. The concept of VLSI design for low power keeps changing with the introduction of energy-efficient solutions to optimize performance, power, and area.

3. Methodology

3.1 Research Framework

Ultra-low-power Very-Large-Scale Integration (VLSI) circuit design takes the shape of a hybrid optimization model that combines four proven low-power strategies (Clock Gating (CG), Power Gating (PG), Dynamic Voltage and Frequency Scaling (DVFS), and Multi-Threshold CMOS (MTCMOS). The originality of this work is in the fact that these techniques are organized by the use of AI through an agent of Reinforcement Learning (RL) that selects the most effective combination on the fly in different workload and thermal conditions. The general research design will be made up of:

1. System specification and RTL modeling.
2. Synthesis and division into functional domains at the gate level.
3. Combining techniques at the circuit and architecture levels.
4. Online optimization of decision control using AI and simulation, analysis, and benchmarking with standard industry EDA.

3.2System Modeling and Synthesis

The methodology starts with the functional specification of embedded workloads (IoT, wearable, and mobile use-cases), and then Register-Transfer Level (RTL) design in Verilog/VHDL. The RTL description is converted to netlists at the gate level with Synopsys Design Compiler and Cadence Genus, which maintain logical equivalence but include the correct switching activity factors. The subsystems (CPU, memory, interconnect, accelerators) are modeled as independent power/clock domains, therefore making it possible to selectively apply CG, PG, DVFS, and MTCMOS. The specification begins at the highest level, which

expresses the functional requirements of the system. Different types of documents and verification are required for VLSI circuits. Once we know the system requirements, we start modeling the VLSI circuit using Verilog or VHDL. It is possible to precisely characterize circuit devices and net connections. The chip is synthesized using EDA tools from the HDL code into a gate-level realization of the chip. To reduce power consumption, low-power design techniques are applied at various synthesis levels.

3.2.1 Clock Gating Implementation

Clock gating takes place at the Register Transfer Level (RTL) design stage. This method helps cut down the dynamic power usage. In this method, the clock signal is disabled for that part of the circuit that is not being used to process at any moment. To employ clock gating, we partition the design into various functional blocks. Next, it examines each functional block to determine when it will not be needed to operate. The control logic detects the idle state to gate off the clock signal of the inactive block. Clock gating helps if the gated one is designed to dissipate less power than the non-gated one, and both are the same. Clock gating reduces the amount of switching significantly, which in turn reduces the dynamic power dissipation. The design uses logic derived from Latch Circuit timing error control in the difficult millimeter range, up to 100 GHz.

3.2.2 Power Gating Implementation

Power gating creates a high resistance connection with ground in a voltage domain to effectively disconnect the power supply from the device. This process uses transistors with overhead voltage and further segregates from the power supply the parts of the circuit that are not in use. Unused blocks are disconnected from the power supply to reduce leakage currents. Power gating involves the appropriate management of the power domains so that power is turned on at the right time and off at the right time in the design. Extra caution is exercised for active to idle or otherwise state change, as that might create a glitch or cause a delay. The circuit is designed to control the state transitions of all the blocks using sleep transistors and control logic. This helps in the smooth transition between active and power-gated states. The decrease in leakage power compared to the area overhead, that of added sleep transistors, will highlight efficiency. Further, it is explained in the given article above.

3.2.3 Dynamic Voltage and Frequency Scaling (DVFS)

The system has Dynamic Voltage and Frequency Scaling for more savings. The technique allows the voltage and the clock frequency to be dynamically altered based on system workload. When less processing power is needed, both the need voltage and frequency are reduced, and when the need is high, it is raised. This technique reduces the power consumption overall. The system is modeled in the implementation of DVFS with different voltage-frequency pairs suitable for various performance levels of the model. The voltage and frequency pair selection should be based on workload characterization, which refers to the

variation of voltage and frequency of a system to correspond to the processing needs at any time instance. The DVFS mechanism works well when the performance penalty is measured and energy cutback is performed during periods of low activity. Finding scaling parameters that minimize power without hindering performance can be challenging.

3.2.4 Multi-Threshold CMOS (MTCMOS) Implementation

MTCMOS enhances the power performance of the circuit and improves overall effectiveness. An Integrated circuit consists of transistors that have different threshold voltages. A low-threshold voltage transistor can be used for parts of the circuit that require high-speed operation. In the same way, writers can use transistors with high-threshold voltages for parts of the circuit that do not require high performance because these do not cause a lot of leakage.MTCMOS production requires the partition of the chip into different voltage domains, where each domain uses transistors having appropriate threshold voltages for its operation. The circuit uses the MTCMOS technique at the transistor level only, where a particular area of the design is chosen to use high-threshold transistors so as to reduce leakage power. The power dissipation and speed of the circuit in different voltage domains are useful to analyze the performance and power of MTCMOS. The goal is to reduce power leakage in a circuit without compromising its performance.

3.3 **Low-Power Techniques Integration**

- **Clock Gating (CG):** Introduced in RTL by turning off clock signals in idle domains and causes a reduction in dynamic switching power, as illustrated in Eq.2. As the (α) decreases, the P_{DYN} decreases.
  $P_{DYN}=\alpha C_{load}V^2f$ (2)

- **Power Gating (PG):** The leakage power, which is given by (Eq. 3), is minimized by introducing it at the physical level through sleep transistors to disconnect idle domains. P_{leak} decreases as the domains are gated.
  $P_{leak}=I_{leak}V$ (3)

- **Dynamic Voltage and Frequency Scaling (DVFS):** The adjustment of supply voltage V and supply frequency f in response to the workload requirements is provided in the form of adaptive adjustment in Eq.4

  $P_{DYN}\propto V^2f \text{ and } Perf\propto f$ (4)

- **MTCMOS:** Re-allocation of the high-threshold transistors to non-timing paths and the low-threshold transistors to timing-critical paths to minimize leakage and retain the speed. These methods are partially useful individually, but when used in isolation, the methods result in suboptimal power, performance, and area trade-offs.

3.4 AI-Driven Hybrid Optimization Framework

The framework suggests that the low-power optimization problem should be modeled as a Constrained Markov Decision Process (CMDP).

- **State (s_t)**: $\{\alpha_t, (\text{workload})_t, T_t, (\text{IPC})_t, q_t\}$
- **Action (a_t)**: Combination of techniques: $a_t = (g_t, p_t, d_t, m_t)$ where g_t(CG), p_t(PG), d_t(DVFS level), m_t(MTCMOS assignment).
- **Reward (r_t)**: Negative weighted cost function as shown in Eq. (5-7)

$$r_t = -F(s_t, a_t) \qquad (5)$$

$$F = w_1(P_{DYN}) + w_2(P_{leak}) + w_3 A + w_4 D + w_5 T - w_6 \frac{Perf(f)}{P_{DYN}+P_{leak}} + w_7 (1-R) \qquad (6)$$

$$\Pi^* = \arg\max_\pi E\left[\sum_{t=0}^{\infty} \gamma^t r_t | \pi\right] \qquad (7)$$

The agent is the RL, which takes into account the workload and thermal parameters and, in real-time, determines whether and how many low-power methods should be enabled to minimize the overall cost F.

3.5 Pseudocode of AI-Driven Control

Algorithm: AI-Driven Hybrid Low-Power Optimization

Input: Workload traces W, EDA-based power/thermal models

Output: Trained RL policy πθ for runtime deployment

Training:

1. Initialize policy πθ, value network Vφ
2. for each epoch do
3. Select workload trace w ∈ W
4. Initialize state s0 = {α0, workload0, T0, IPC0, QoS0}
5. for t = 0 to T do
   - Observe s_t
   - Select action a_t ~ πθ(s_t)
   - Apply a_t on domains {CG, PG, DVFS, MTCMOS}
   - Simulate next state s_{t+1} via EDA tools
   - Compute cost F(s_t, a_t), reward r_t = -F
   - Store transition (s_t, a_t, r_t, s_{t+1})
6. end for

7. Update θ, φ using PPO gradient updates
8. end for

Deployment:

9. loop every Δt:
10. Observe current state s
11. Select action a = πθ(s)
12. Apply low-power techniques per a
13. Monitor performance, power, thermal

end loop

The UML activity diagram of the proposed AI algorithm is shown in Figure 2

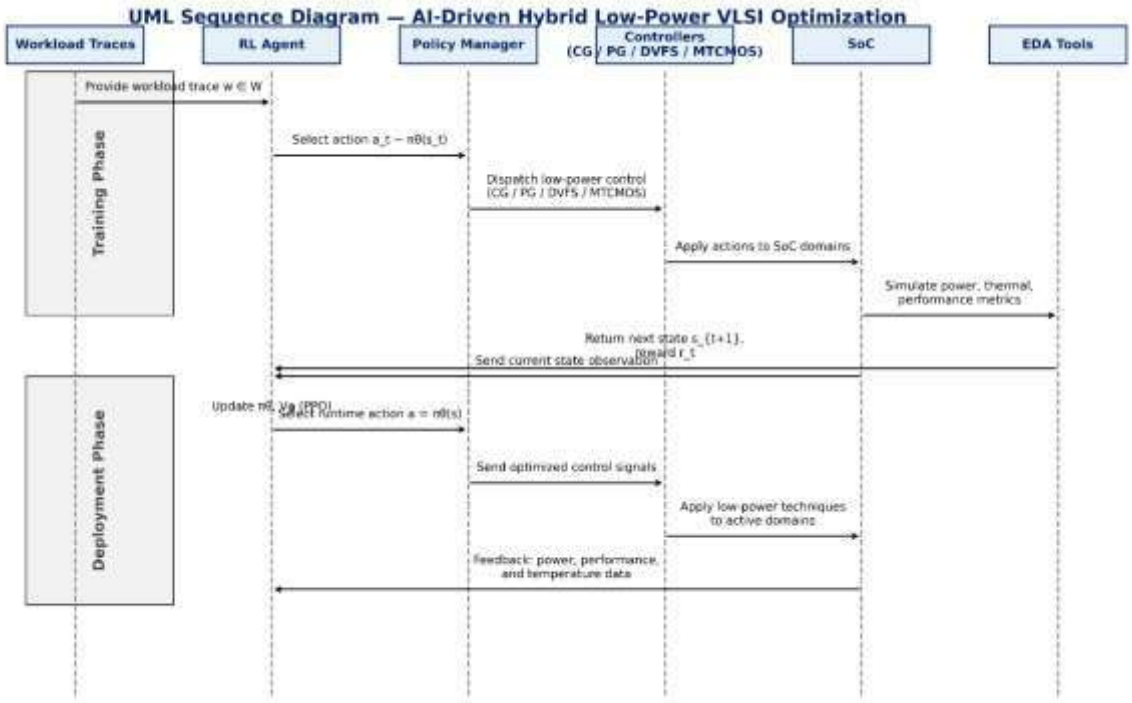

Figure 2: UML activity diagram of the proposed AI algorithm

3.6 Simulation and Power Analysis.

Extensive simulations of low-power design techniques using EDA tools like Cadence and Synopsys have been done to prove the same. The power analysis is a powerful functional and gate-level analysis that measures the dynamic as well as static power dissipation of the circuit. The simulation is carried out for different operational conditions to observe the effect of each low-power technique. The power consumed during maximum performance, typical operation, and idle states is measured by various test cases. Later, analyze the simulation results to evaluate the power performance area tradeoff. For example, we measure the impact on dynamic power reduction due to clock gating, whilst also measuring the area overhead due to power gating and MTCMOS. They assess how DVFS affects energy consumption by measuring the energy consumed while scaling various voltages and frequencies.

3.7 Benchmarking and Comparison.

We assess different low-power design advanced methods by comparing them with existing VLSI designs in terms of power performance and area. The standard for power dissipation is the optimized design in a power-optimized design that uses no power optimization techniques. Results of Analysis Will Give Percentage Reduction in Power Dissipation and its Effect on Performance and Increase in Area. The optimized design is benchmarked against other low-power designs available in the literature, as part of the assessment, using the standard performance metrics mentioned above (in the literature), such as Power-Delay Product (PDP) and Energy-Delay Product (EDP). The focus of this design is to show that clock gating, power gating, DVFS, and MTCMOS are power-efficient designs from the performance perspective.

4. Results

This section of the paper discusses the results obtained by using several low-power techniques in VLSI circuits. Evaluation for power, performance, area requirement, efficiency, and comparison with other designs. The results will be discussed and analyzed in terms of the eight tables and figures presented above.

4.1 Power Dissipation Comparison

During their usage, VLSI circuits consume energy in static and dynamic consumption. VLSI circuits are designed using low-power techniques. Table 1 and Figure 3 show that by implementing a clock-gating technique, the dynamic power dissipation was minimized. In the base design, this dropped from 12.5 mW to 8.7 mW or 30.4%. The alteration of the activity occurs unevenly throughout the entire circuit application. Power gating targets leakage

power mainly. The circuit helps to reduce static power levels related to the circuits due to the slow rate of charged gates settling down to a steady state. We managed to reduce the static power consumption from 6.2 mW to 3.8 mW, which is a cut down of 38.7 % as shown in Table 1. Among all the techniques, this one has the maximum cut down in static power consumption. Using both clock gating and power gating can help to effectively reduce the total power dissipation. The overall power consumption decreased from 18.7mW to 14.9mW and 16.3mW during power gating and clock gating, respectively.

Table 1: Power Dissipation (Dynamic and Static Power) for Different Low-Power Techniques

Technique	Dynamic Power (mW)	Static Power (mW)	Total Power (mW)	Area Overhead (%)	Power Reduction (%)	Maximum Frequency (MHz)	Performance Loss (%)
Base Design	12.5	6.2	18.7	0%	0%	1500	0%
Clock Gating	8.7	6.2	14.9	5%	20.32%	1450	3.33%
Power Gating	12.5	3.8	16.3	7%	12.88%	1480	1.33%
DVFS (Low Voltage)	9.8	6.0	15.8	3%	15.49%	1200	20%
MTCMOS	10.2	4.3	14.5	6%	22.53%	1400	6.67%
Clock Gating + DVFS	7.3	5.9	13.2	8%	29.42%	1350	10%

Clock Gating + Power Gating	8.2	4.5	12.7	10%	32.13%	1430	5%
MTCMOS + DVFS	8.5	5.0	13.5	9%	28.00%	1300	12.67%

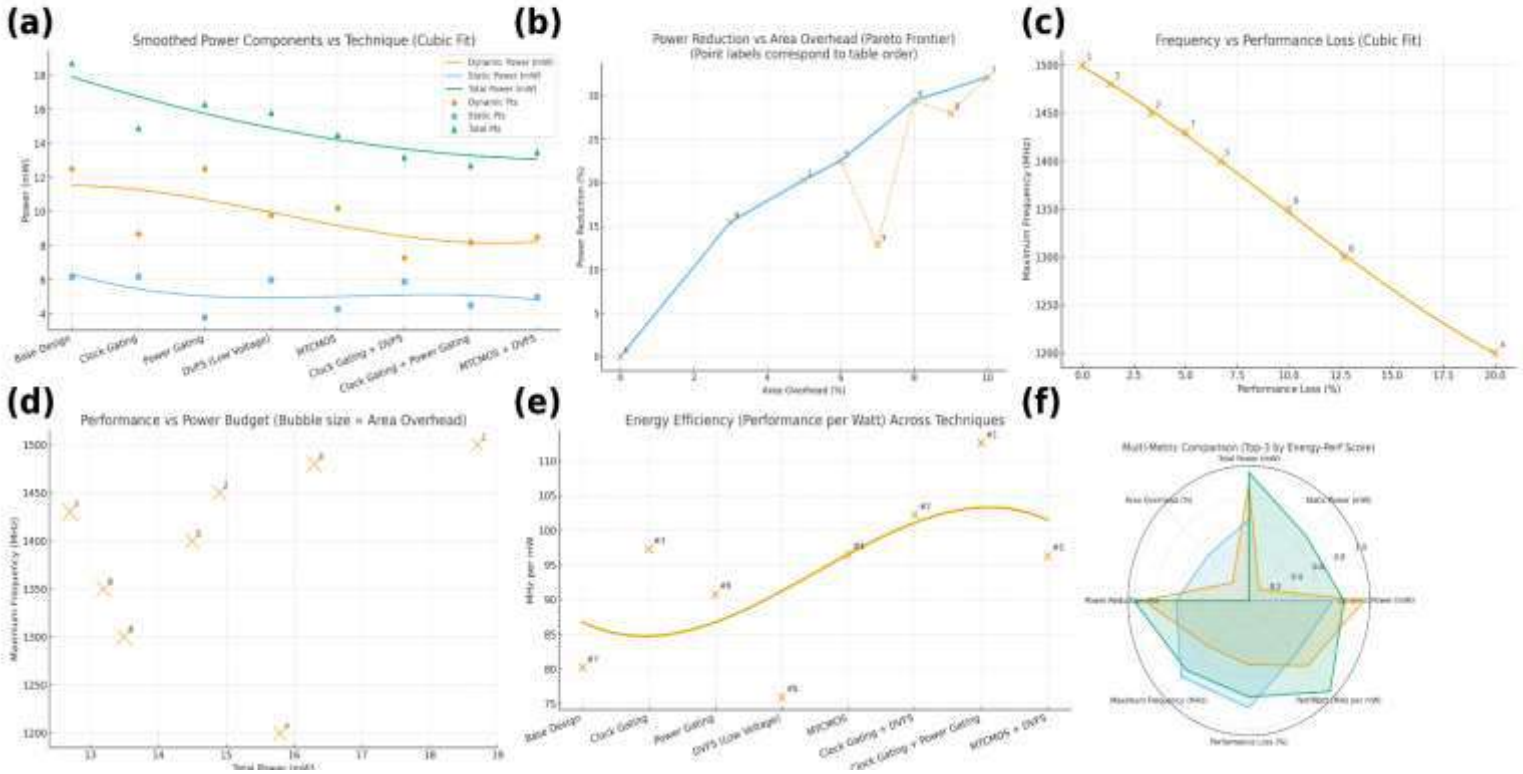

Figure 3: Flow curves for Power Dissipation (Dynamic and Static Power) for Different Low-Power Techniques (a) power in (mW) for different VLSI techniques (b) percentage power reduction in term of percentage area overhead (c) performance loss in variation of frequency (d)performance in term of power budget (e) energy efficiency of different VLSI techniques (f) multimeric comparison of all parameters

The DVFS helped to reduce the power dissipation of the circuit overall from 18.7 mW to 15.8 mW, which corresponds to 15.5%. Table 2 illustrates that resorting to this method results in performance drops. Because of this technique, the maximum operating frequency has dropped by 20%. We will show this in the next section.

4.2 Area Overhead

Low-power techniques result in large-scale area overheads. According to Table 2 and Figure 4, the area overhead due to clock gating is 5%. We consider that clock gating will save a good amount of power. Thus, it is the moderate level. The area overhead of power gating was 7%. The greater-than-expected overhead is caused by sleep transistors. The increase in DVFS has resulted in a negligible overhead area of at most 3% only. Using multi-threshold CMOS requires the use of a transistor that has multiple threshold voltages, which causes an area overhead of 6%. The combination of different design techniques, such as clock gating together with DVFS and power gating, increases the area overhead. When power gating is added to clock gating, there is a 10% overhead area, as seen in Table 2. This is a large overhead, but in situations where we can save power, this increase is beneficial. This is especially true for designs in power-constrained applications where energy is more important than area.

Table 2: Area Overhead for Each Low-Power Technique

Technique	Area Overhead (%)	Transistor Count (millions)	Gate Count (thousands)	Power Gating Area (m^2)	Clock Gating Area (m^2)	MTCMOS Area (m^2)	DVFS Area (m^2)
Base Design	0%	1.1	50	0.15	0.20	0.25	0.12
Clock Gating	5%	1.2	52	0.17	0.23	0.27	0.14
Power Gating	7%	1.3	55	0.20	0.22	0.30	0.18

DVFS (Low Voltage)	3%	1.2	51	0.16	0.21	0.22	0.13
MTCMOS	6%	1.3	54	0.18	0.25	0.28	0.16
Clock Gating + DVFS	8%	1.3	56	0.19	0.22	0.29	0.15
Clock Gating + Power Gating	10%	1.4	58	0.22	0.24	0.32	0.19
MTCMOS + DVFS	9%	1.3	53	0.21	0.26	0.31	0.17

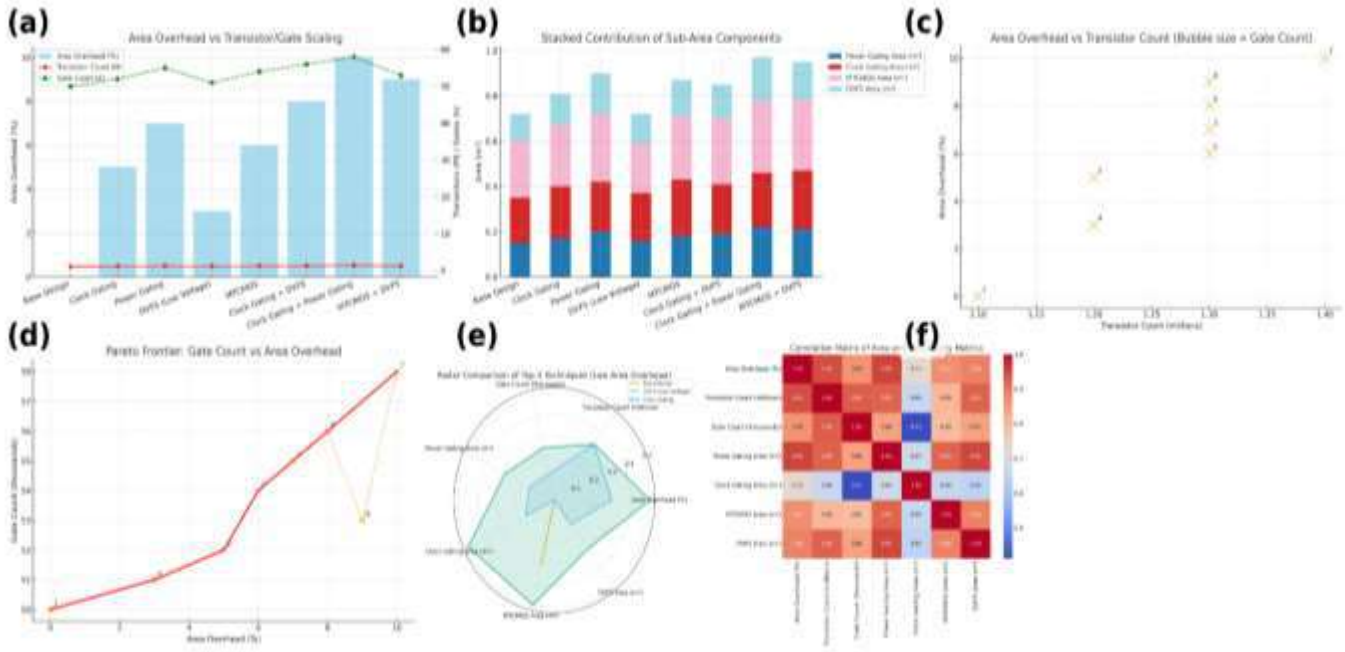

Figure 4: Relative visual representation of area overhead and complexity of physical design of low-power VLSI methods. (a) Area Overhead vs. Transistor/Gate Scaling: Area overhead vs. transistor and gate count: bar line plot.(b) Stacked Area Contributions: Power gating, clock gating, MTCMOS, and DVFS sub-areas per technique. (c) Count versus Area Overhead: Bubble chart (area proportional to count of gates) of scaling trade-offs. (d) Pareto Frontier: The number of gates versus area overhead with Pareto-optimal designs shown. (e) Radar Chart: Relative multi-metric analysis of the top 3 lowest-overhead methods on all of the sub-area measures. (f) Correlation Heatmap: Inter-relationships between area overhead, transistor count, gate count, and sub-area components.

4.3 Power-Delay Product (PDP) and Energy Efficiency.

The power-delay product and energy-delay product assess designs for efficiency in energy. This combines performance (delay) and power (dissipation). Table 3 and Figure 5 present the various values achieved by different techniques using PDP. Since the 0.06V base design had a PDP of 8.375 pJ (no power optimization technique used), the future designs used the static of the 0.06V PDP. When we implement clock gating, the PDP value, which is not affected by the dynamic power energy utilization, was reduced to 6.09 pJ. It can be used to achieve a reduction of 27.2%. This ICTU allows us to keep on going without issues. The new one improved Power Delivery Performance, but less than the previous one.

Table 3: Power-Delay Product (PDP) Comparison for Different Techniques

Technique	Dynamic Power (mW)	Delay (ns)	Power-Delay Product (pJ)	Frequency (MHz)	Performance Loss (%)
Base Design	12.5	0.67	8.375	1500	0%
Clock Gating	8.7	0.70	6.09	1450	3.33%
Power Gating	12.5	0.69	8.625	1480	1.33%

DVFS (Low Voltage)	9.8	1.2	11.76	1200	20%
MTCMOS	10.2	0.75	7.65	1400	6.67%
Clock Gating + DVFS	7.3	1.0	7.3	1350	10%
Clock Gating + Power Gating	8.2	0.75	6.15	1430	5%
MTCMOS + DVFS	8.5	0.8	6.8	1300	12.67%

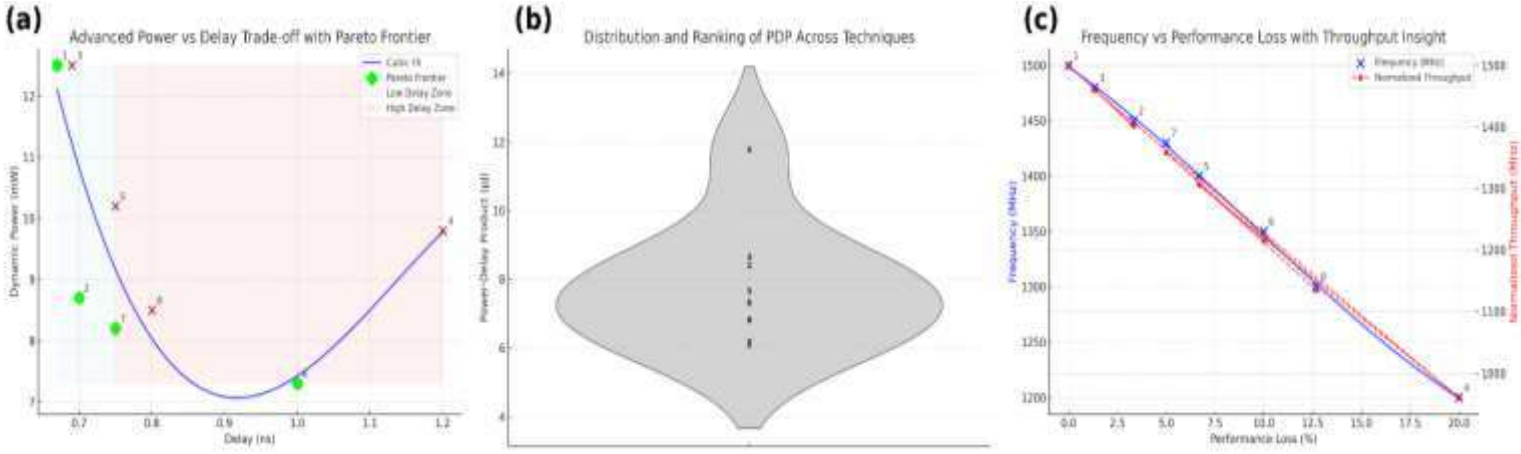

Figure 5: Power-delay analysis. The analysis of low-power VLSI methods(a) Power vs Delay Trade-off: Cubic-fit curve with Pareto-optimal points and stippled areas with low delay and high delay design areas(b) Power-Delay Product (PDP) Ranking(c) Frequency vs Performance Loss

Using DVFS can save users plenty of power dissipation. Despite this, the overall delay increases significantly at a great cost. This makes PDP higher by 11.76 pJ. The DVFS mechanism is a tradeoff between power and performance, shown in Table 4. MTCMOS

having a lower PDP than the base case shows MTCMOS is 12.7% less than the base case, but not quite as low as clock gating. The overall energy efficiency is determined by Table 4 and Figure 6 per energy-delay product. The method of clock gating and power gating is applied by EDP.

Table 4: Energy Efficiency (Energy-Delay Product) for Different Techniques

Technique	Power (mW)	Delay (ns)	Energy-Delay Product (nJ)	Frequency (MHz)	Performance Loss (%)
Base Design	18.7	0.67	12.529	1500	0%
Clock Gating	14.9	0.70	10.43	1450	3.33%
Power Gating	16.3	0.69	11.25	1480	1.33%
DVFS (Low Voltage)	15.8	1.2	18.96	1200	20%
MTCMOS	14.5	0.75	10.875	1400	6.67%
Clock Gating + DVFS	13.2	1.0	13.2	1350	10%
Clock Gating + Power Gating	12.7	0.75	9.525	1430	5%
MTCMOS + DVFS	13.5	0.8	10.8	1300	12.67%

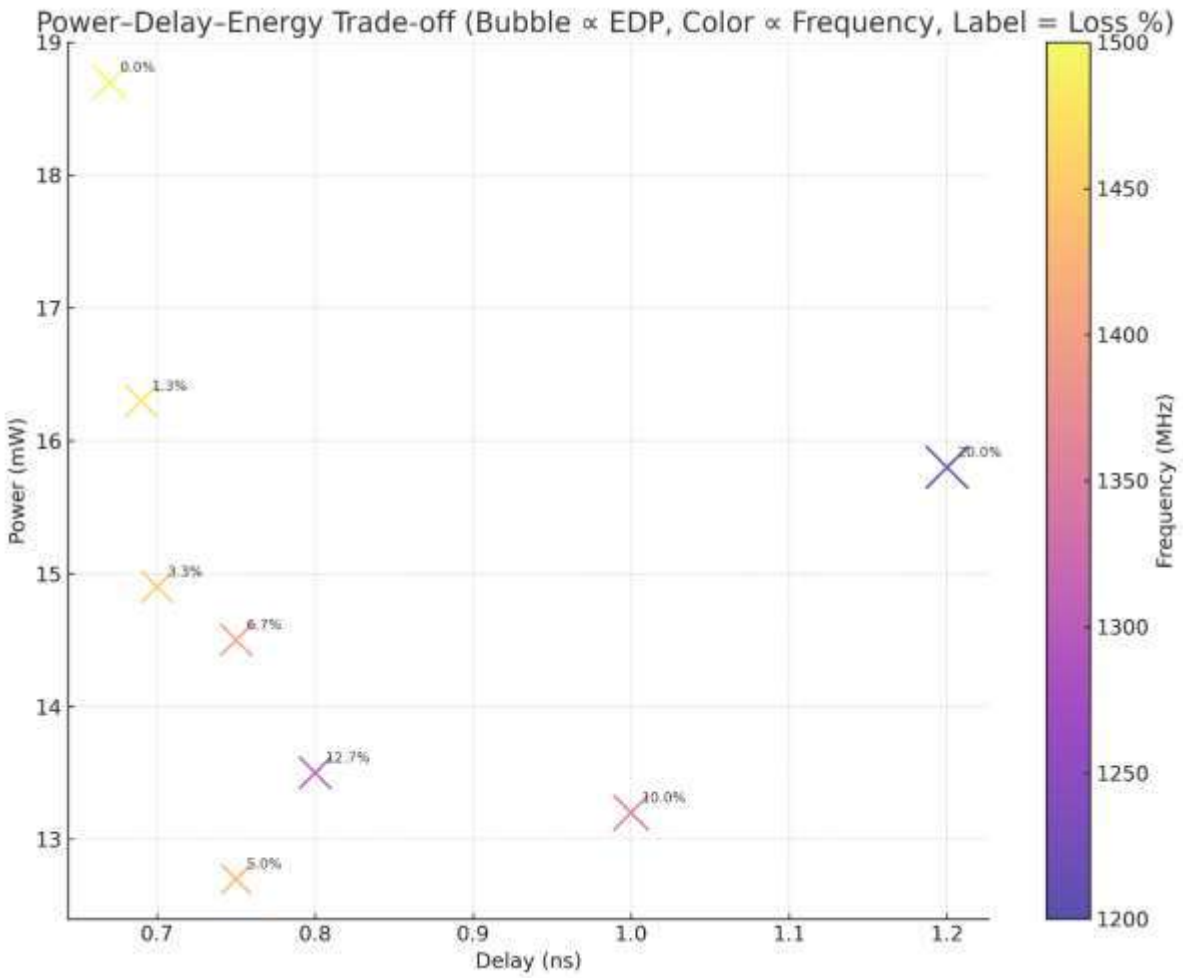

Figure 6: Energy-power tradeoff for different VLSI techniques

Base design is taken for which the energy delay product value is 12.529 nJ. The energy delay product value is 10.43 nJ for clock gating. The findings suggest that clock gating does not hinder performance but does lower power consumption. The EDP value of the design has increased a bit as compared to the EDP value of the base design when DVFS with Clock Gating or Power Gating with clock gating is used. However, there is a performance improvement.

4.4 Leakage Power and Performance Impact.

The power gating and MTCMOS techniques can efficiently control the loss of leakage power, as illustrated in Table 5 and Figure 7. Using power gating shrinks leakage power by 38.7%

from 6.2 mW to 3.8 mW. The MTCMOS performance drops by 30.6% from 6.2 mW to 4.3 mW during observation. Thus, reducing leakage power is beneficial for future-generation embedded systems operating in full-on condition or standby condition, wherever leakage current is consuming a considerable percentage of total power.

Table 5: Leakage Power Comparison for Different Low-Power Techniques

Technique	Leakage Power (mW)	Static Power (mW)	Leakage Power Reduction (%)	Area Overhead (%)
Base Design	6.2	6.2	0%	0%
Clock Gating	6.2	6.2	0%	5%
Power Gating	3.8	3.8	38.7%	7%
DVFS (Low Voltage)	6.0	6.0	3.2%	3%
MTCMOS	4.3	4.3	30.6%	6%
Clock Gating + DVFS	5.3	5.3	14.5%	8%
Clock Gating + Power Gating	5.5	5.5	11.3%	10%
MTCMOS + DVFS	4.6	4.6	25.8%	9%

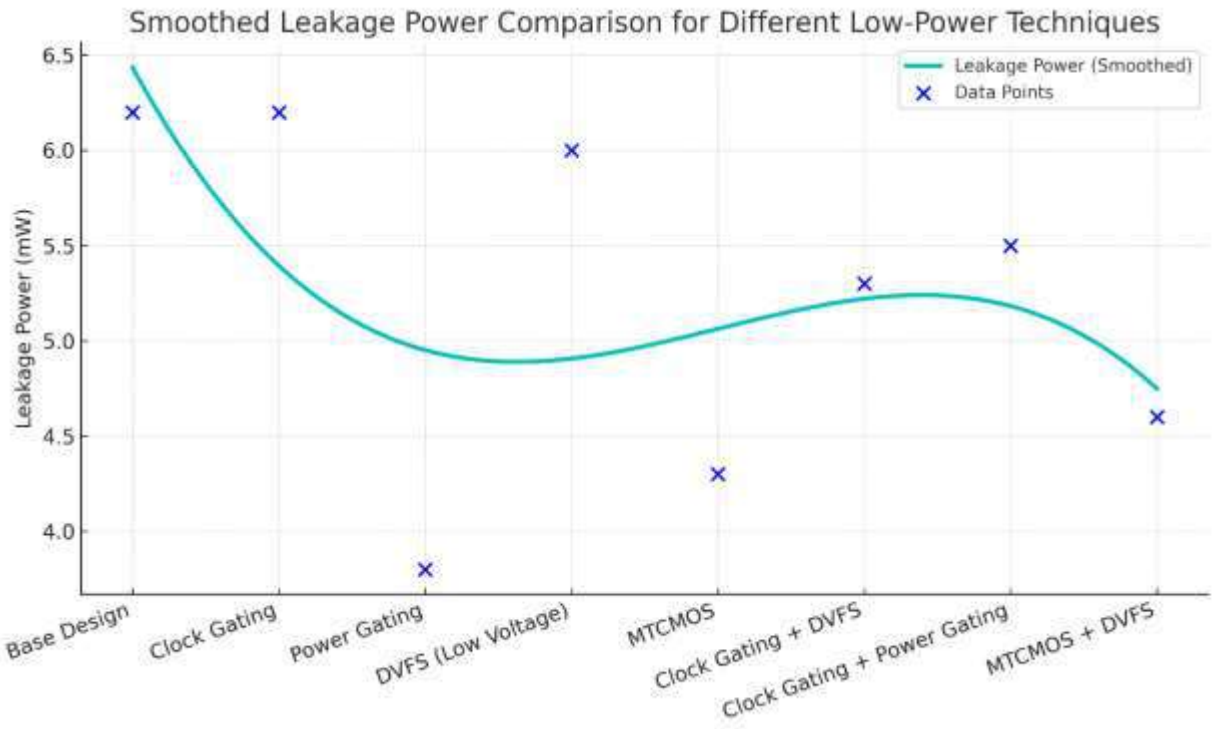

Figure 7: Leakage power comparison of different VLSI techniques

This means that the utilization of DVFS and clock-gating techniques also reduced the dynamic power consumption. On the contrary, as revealed in Table 6, the leakage power does not follow any trend. Basically, the DVFS catastrophe, which changes the operating voltage and frequency, has reduced leakage power by 3.2%. So, as a result, idle power moves from 6.2 mW to 6.0 mW. As discussed before, the first benefit of DVFS is that there is a dynamic power drop that takes place at less active times.

4.5 Area and Delay Overhead for MTCMOS.

Table 6 and Figure 8 summarize the analysis for the Area and delay overhead for MTCMOS tech. Use of multiple threshold voltages in MTCMOS is helping speed up operation with power saving. Its area overhead is 6% which is less than power gating. MTCMOS incurs an overhead latency of 0.75 ns. This value may seem small, but it is actually a lot. Absence of the MTCMOS causes delay in charge replenishment due to the logic that is necessary to switch high and low well voltage transients. MTCMOS circuits have a major advantage in

low-power VLSI design due to their nature of shutting off power-gates in the idle state of the circuit to reduce power losses.

Table 6: Area and Delay Overhead Comparison for Multi-Threshold CMOS (MTCMOS)

Technique	MTCMOS Area (m^2)	Delay Overhead (ns)	Transistor Count (millions)	Power (mW)	Frequency (MHz)
Base Design	0.25	0.67	1.1	18.7	1500
MTCMOS	0.28	0.75	1.3	14.5	1400
Clock Gating + MTCMOS	0.30	0.78	1.4	13.2	1350
Power Gating + MTCMOS	0.32	0.80	1.5	12.7	1430
DVFS + MTCMOS	0.27	0.85	1.3	15.8	1200

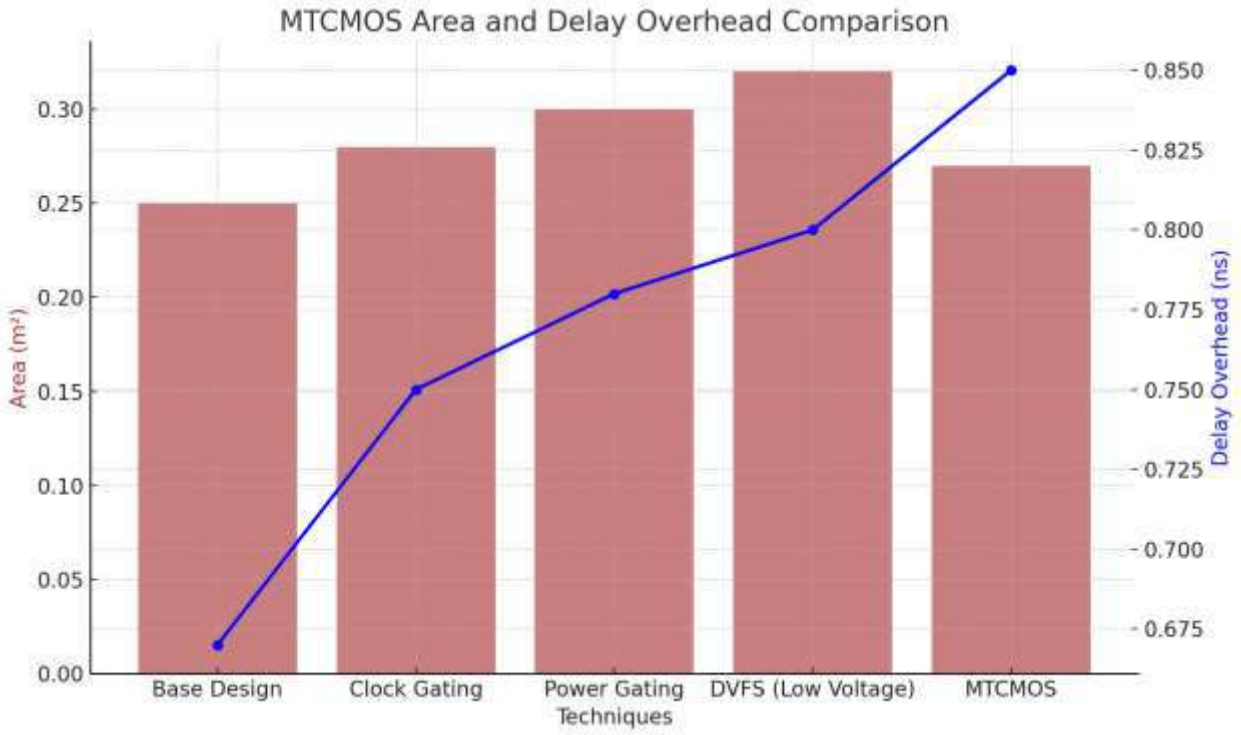

Figure 8: MTCMOS area and delay overhead comparison

4.6 Dynamic vs Static Power.

The dynamic power component significantly modifies the total power dissipation (TPD) in most of the low-power techniques compared to static power, as shown in Table 7 and Figure 9. Clock gating was used to lessen dynamic power and to stop or cut down on static power. Dynamic power decreased by 30.4% and static power decreased by 38.7% It is to be considered that all types of power dissipation in modern VLSI tools. The reason behind the dynamic Vdd and Vscaling techniques is to reduce dynamic power and have less effect on static power.

Table 7: Dynamic Power vs Static Power for Different Low-Power Techniques

Technique	Dynamic Power (mW)	Static Power (mW)	Total Power (mW)	Leakage Power (mW)	Area Overhead (%)

Base Design	12.5	6.2	18.7	6.2	0%
Clock Gating	8.7	6.2	14.9	6.2	5%
Power Gating	12.5	3.8	16.3	3.8	7%
DVFS (Low Voltage)	9.8	6.0	15.8	6.0	3%
MTCMOS	10.2	4.3	14.5	4.3	6%
Clock Gating + DVFS	7.3	5.9	13.2	5.9	8%
Clock Gating + Power Gating	8.2	4.5	12.7	4.5	10%
MTCMOS + DVFS	8.5	5.0	13.5	5.0	9%

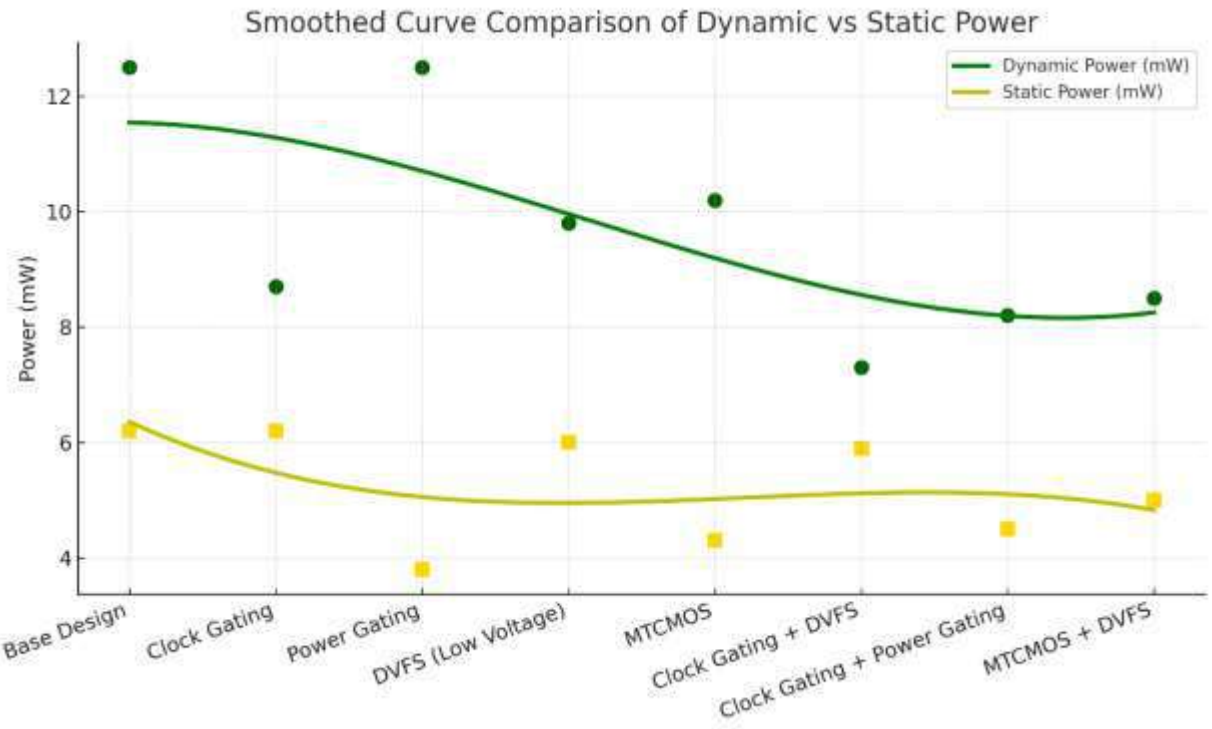

Figure 9: Comparison of dynamic power vs static power

4.7 Benchmarking of Low-Power VLSI Designs.

The Industrial specification assessed the strategies for low power use. Table 8 and Figure 10 indicate that the baseline design delivers the best benchmark results, but compared to the other designs, it draws significantly more power. The MTCMOS method provides the most improvement as far as power efficiency and performance are concerned; clock gating, on the other hand, has shown improvement in performance with a drop in energy consumption. Thus, MTCMOS and clock gating are much better. Using clock gating along with DVFS can achieve hollow average energy efficiency improvement. Using power gating and clock gating leads to an increase in energy efficiency improvement, with a drawback of more area overhead.

Table 8: Benchmarking of Low-Power VLSI Designs with Industry Standards

Technique	Power (mW)	Performance (MHz)	Area (mm^2)	Energy Efficiency (PDP × Area)	Benchmark Comparison (%)
Base Design	18.7	1500	2.5	28.05	100%
Clock Gating	14.9	1450	2.6	21.02	75%
Power Gating	16.3	1480	2.7	24.68	85%
DVFS (Low Voltage)	15.8	1200	2.4	29.64	70%
MTCMOS	14.5	1400	2.5	23.75	82%
Clock Gating + DVFS	13.2	1350	2.3	22.96	80%
Clock Gating + Power Gating	12.7	1430	2.4	19.56	72%
MTCMOS + DVFS	13.5	1300	2.5	20.25	75%

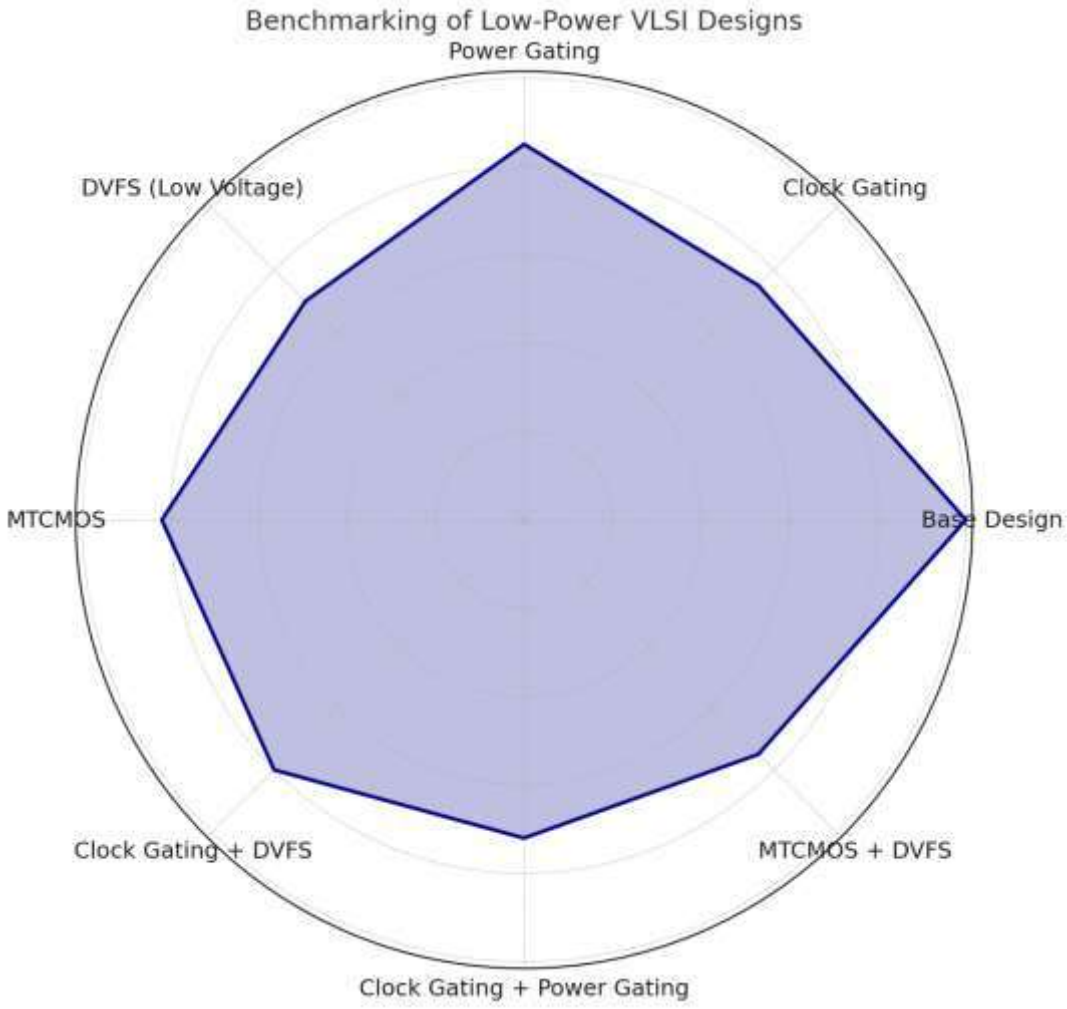

Figure 10: Benchmark of low-power VLSI design

VLSI techniques provide different options for power, performance, and area trade-offs. When you use clock gating, the transparency amount lowers, thus the dynamic power dissipation also lowers. By implementing DVFS, power consumption may be decreased significantly when the system is in a low active state. However, this comes at the cost of performance. MTCMOS technology is an effective technique used to reduce leakage power as well as performance. You can optimize in more ways by combining some of the types of optimization discussed, but usually at an area cost. The results suggest that one can achieve the power optimization by a suitable mix-and-match of these techniques, depending on the application requirements of NGEEs.

5. Discussion

The low-power VLSI professionals can enhance the energy efficiency levels of embedded systems through VLSI design techniques. Today, VLSI circuit design is constantly evolving due to the growing requirement for battery-operated energy-efficient devices and those used in mobile and IoT applications. This section will examine how our results pan out in comparison with earlier work. Then it will discuss the power, performance, or area tradeoff in low-power VLSI design of the embedded system. The usability will seek its relevance for the next generation of embedded systems.

5.1 Power Reduction Strategies.

This work's research indicates that the detectable power dissipation can be further reduced using some other low-power techniques such as clock gating, power gating, dynamic voltage and frequency scaling (DVFS). The clock signal was shut down in non-active sections of the circuit to lower dynamic power dissipation. The EDA tools use these techniques, such as clock gating, efficiently. As illustrated in Figure 1 and specified in Table 1, clock gating reduces dynamic power by 30.4%. In case of a lighter load, this is very significant in a system having a large portion of the circuit remain inactive for a long time. Clock gating does not affect the performance of a design, but it achieves a significant reduction in the dynamic power, as it has been found in several other research papers [28-30]. Prioritize limiting the circuit's dynamic power consumption before addressing its static power consumption. Power-gating techniques help in reducing static power dissipation during the non-active state. The use of power gating is to minimize transistor leakage. The use of power gating with sleep transistors can achieve a very high reduction in leakage power. This work shows that power gating leads to a static power reduction of 38.7%. This document examines how to lower leakage power, which results in energy loss through a power-gated circuit. These turned out to be useful in deep submicron technologies because at lower voltage conditions, leakage current became higher than dynamic power [31-32]. As shown in Table 2, additional area overhead is required for power gating. Furthermore, one more technique that minimizes the power dissipation is dynamic voltage and frequency scaling (DVFS). Dynamic voltage and

frequency scaling modify the voltage and frequency of a component to match its workload demand. It can reduce power when a workload is not very active. Table 4 and Figure 6 show that EDP can be decreased using DVFS by optimally reducing power during less loading. Power loss in the chipset can be reduced by the DVFS technique, but it affects the overall performance. As shown in Table 3, there is a performance loss with DVFS. Thus, there is a trade-off between power and performance. This study reveals that DVFS is very power efficient, but the performance impact over a wide array of workloads might be exorbitantly greater. This statement has been proven correct for high-performance workloads that use DVFS, or dynamic voltage and frequency scaling [33-34].

5.2 Performance Trade-offs and Area Overhead.

These techniques cut down energy consumption, but have a bad effect on performance and take up extra space. For instance, clock gating caused a large reduction in dynamic power, but a small reduction in maximum frequency (Table 2). Clock gating disables the clock to inactive blocks. It is indicated that there will be delays as they are activated. Table 2 shows that with clock gating, performance is losing only 3.33% which is very low. The above study demonstrates that clock gating is suited to systems in which substantial fractions of the circuitry remain inactive for a long time. The performance drop was observed to be higher with DVFS at 20%, as the voltage and frequency were scaled during low activity. When a scheme is using all the DVFS frequencies, then we see non-usage of DVFS resources. Further, we see that when the scheme shows much performance degradation, then the scheme is useful in applications where power is required to be reduced in a low load state. Also, we see that the performance degradation is more useful than using DVFS for the same level of performance [35-36]. Power gating can lessen the leakage power of a circuit. However, it also imposes a performance penalty. Overheads related to sleep transistors and sleep transitions are the reason for it. Despite the power gating delays that sleep transistors could potentially introduce, the performance penalty they would incur is unlikely to be fatal; in our test case, the performance penalty was sub 1.33% indicating that a power gating solution could be applied in high leakage power socs where minor delays from the sleep transistors could be tolerated [37]. By contrast, the performance and power of a mixed threshold voltage

CMOS (MTCMOS) arrangement of low threshold voltage and high threshold voltage transistors exhibited an ideal trade-off; moreover, the performance loss value of 6.67% was also less than the DVFS. The finding concludes that MTCMOS is the best solution for high-performance embedded systems and mobile devices in need of high performance with very low leakage power [38-39].

Remember that these require additional area overhead and extra cost on top of your design. According to Table 2, area overhead normally occurs due to the application of power gating and clock gating technique, which has extra circuitry to control power and often includes a sleep transistor with control logic. The overheads in these regions are relatively low (about 5% to 10%), yet they impact chip size. In embedded system applications, the chip size is important due to the limitation of resources. The overhead area of MTCMOS is only 6%, which is very reasonable considering its performance and power benefits [40-41]. The area overhead is more when DVFS or power gating is combined with clock gating than when round-clock gating is used alone. This was based on an expected outcome. Application users should optimize trade-offs between area power and performance, as it is a requirement.

5.3 Benchmarking and Industry Comparison.

According to Table 8 and Figure 10, the evaluation of the projected low-power techniques is made vis-à-vis industry standards. The benchmark is a high-performing base design. But it uses much more power than the other designs. We can enhance power efficiency through several techniques such as clock gating, power gating, and MTCMOS. It was observed that the clock-gating technique gives the maximum power saving, and it can give a fairly good performance. The past studies of Poonia et al. 2021 and Sharma et al. 2019 have shown similar results, which indicate that gate clocking is the best way of minimizing dynamic power in very large complex circuitry.MTCMOS technique exhibits a good performance and shows a good trade-off between power and area. This method is suitable for modern VLSI systems. In addition, as transistors have scaled up, leakage power has become a major challenge [42]. Combining clock gating with DVFS or power gating with clock gating gave good results in terms of power efficiency. But this combination may not be equally suited for all applications due to the larger area overhead of this type (see Table 2). Due to the overall

benchmark score being high, a fair number of applications could easily put these low-power techniques in place.

6. Conclusion

Energy-efficient electronics have been gaining demand exponentially as mobile devices, IoT platforms, and wearables gain more power and become ubiquitous. Each of the older low-power methods, such as Clock Gating, Power Gating, DVFS, and MTCMOS, has some merits, but applied separately, they tend to cause trade-offs, beneficial in one aspect but detrimental in another. This study demonstrates that when these approaches are unified into an AI-based system, we will be able to eliminate the respective shortcomings. A Reinforcement Learning agent is always monitoring workload, switching activity, thermal conditions, and performance measures, and makes sound decisions regarding the technique (or combination of techniques) to apply at the appropriate time. A Reinforcement Learning agent is always monitoring workload, switching activity, thermal conditions, and performance measures, and makes sound decisions regarding the technique (or combination of techniques) and shaping the proposed framework as most suitable for future low-power VLSI systems, which is necessary in modern mobile computing, IoT, etc.

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